20EC4210

	Reg. No:		
	SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY ··· P		
	(AUTONOMOUS)	UTIUK	
	M.Tech I Year II Semester Regular Examinations November-2	021	
	LOW POWER VLSI DESIGN		
	(VLSI Design)		
	Time: 3 hours	Max. M	Marks: 60
	(Answer all Five Units 5 x 12 = 60 Marks) UNIT-I		
1	a Explain about Silicon-on-Insulator (SOI) technology.	L1	6M
	b Explain in detail about threshold voltage adjustment for CMOS devices.	L3	6 M
2	OR		
4	b How the bipolar transistor takes important role in Isolation in DiCMOS2	L2	6M
	UNIT-II	LI	6 IVI
3	a Explain in detail about copper Electroplating/Copper-Fill.	L1	6M
	b What are the future trends and directions in CMOS/BICMOS processes? Explain OR	n. L2	6M
4	a Describe the device structure and fabrication process for lateral BJT on SOI.	L1	4M
	 b Explain the following Advanced MOSFET models, i) HSPICE level 50 Model ii) EKV MOSFET Model. 	L3	8M
5	a Explain the following parameters in conventional CMOS logic gates,	L1	6M
	 b Explain the following parameters in ESD-free BiCMOS Digital circuits, i) Circuit operation. ii) Comparative evaluation. 	L2	6M
6	a Describe the basic driver configuration in conventional Bi CMOS logic gates.	L2	6M
	b What are all the performance evaluation and comparison of BiCMOS logic gates	s? L1	6 M
7	a Explain about the pipelining theme in the evolution of Latches and Flip-flop.	L2	6M
	 b Explain in detail about Dynamic flip-flops in single edge-triggered Flip-flops. OR 	L1	6M
8	a Discuss about the sensitivity to clock skew and input and clock skew rate of performance measures for latches and Flip-flop.	L1	6M
	b Explain about the high performance and low power theme in the evolution of lat and Flip-flop.	ches L2	6M
0	UNIT-V		
ሃ	a now the swing clock is used to reduce the power in clock networks? b Discuss Tristate Keeper Circuit in CMOS Election No.1	L1	6M
	OD	L3	6M
10	Describe the Oscillator Circuit for Clock Generation.	L1	12M

R20

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